



PATENT
Docket No.: 02207/10607

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

APPLICANTS: Solomon et al.
SERIAL NO.: 09/892,566
FILED: June 28, 2001
FOR: POWER REDUCTION FOR PROCESSOR FRONT-END BY
CACHING DECODED INSTRUCTIONS
ART UNIT: 2188
EXAMINER: Gary J. Portka

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 CFR § 1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom. The filing of this Information Disclosure Statement and the enclosed PTO Form No. 1449, shall not be construed as an admission that the information cited is prior art, or is considered to be material to patentability as defined in 37 C.F.R. § 1.56(b). The paragraphs marked below are applicable. It is believed that no fees other than those indicated below are due, but authorization is hereby given to charge any additional fees due, or to credit any overpayment, to deposit account 11-0600.

■ 1. This Information Disclosure Statement is being filed (a) within three months of the filing date of a national application other than a continued prosecution application under 37 C.F.R. §1.53(d), (b) within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, (c) before the mailing date of a first Office Action on the merits in the present application, OR (d) before the mailing of a first office action after filing of a request for continued examination. No certification or fee is required.

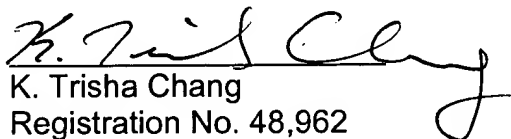
☐ 2. This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a final action, Notice of Allowance, or any action that otherwise closes prosecution.

■ 3. The Examiner's attention is directed to co-pending U.S. Patent Application No. 09/961,202, filed September 24, 2001, and co-pending U.S. Patent Application Serial No. 09/735,899, filed December 14, 2000, which are directed to related technical subject matter. The identification of these U.S. Patent Applications is not to be construed as a waiver of secrecy as to that application now or upon issuance of the present application as a patent. The Examiner is respectfully requested to consider the cited applications and the art cited therein during examination of the present application.

Respectfully submitted,

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Date: November 22, 2004


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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known

Application Number	09/892,566
Filing Date	June 28, 2001
First Named Inventor	B. Solomon et al.
Art Unit	2188
Examiner Name	Gary J. Portka
Attorney Docket Number	02207/10607

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
		US-6,507,921	01-14-03	Buser et al.	
		US- 6,351,844	02-2002	Bala	
		US- 6,339,822	01-15-02	Miller	
		US- 6,279,103	08-21-01	Warren	
		US- 6,233,678	05-15-01	Bala	
		US- 6,216,200	04-10-01	Yeager	
		US- 6,189,140	02-13-01	Madduri	
		US- 6,185,675	02-06-01	Kranich et al.	
		US- 6,076,144	06-2000	Peled et al.	
		US- 6,073,213	06-2000	Peled et al.	
		US- 5,974,538	10-26-99	Wilmot II	
		US- 5,966,541	10-12-99	Agarwal	
		US- 5,924,092	07-1999	Johnson	
		US- 5,889,999	03-30-99	Breternitz, Jr., et al.	
		US- 5,461,699	10-24-95	Arbabi et al.	
		US- 4,575,814	03-11-86	Brooks, Jr., et al.	
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	English Abstract
		Country Code ³ - Number ⁴ - Kind Code ⁵ (if known)				

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 2 of 2

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First Named Inventor	B. Solomon et al.
Art Unit	2188
Examiner Name	Gary J. Portka
Attorney Docket Number	02207/10607

NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Conte et al, "Optimization of Instruction Fetch Mechanisms for High Issue Rates," <i>Proceedings of the 22nd Annual Int'l. Symposium on Computer Architecture</i> , June 22-24, 1995, Santa Margherita Ligure, Italy, pp. 333-344	
		Dutta et al, "Control Flow Prediction with Tree-Like Subgraphs for Superscalar Processors," <i>Proceedings of the 28th Int'l. Symposium on Microarchitecture</i> , Nov. 29-Dec. 1, 1995, Ann Arbor, MI, pp. 258-263.	
		Hennessy et al., <i>Computer Organization and Design: the hardware/software interface</i> , 2 nd Edition, Morgan Kaufmann Publishers, San Francisco, CA, 1998, p. 570.	
		Johnson, Mike, <i>Superscalar Microprocessor Design</i> , PTR Prentice-Hall, Englewood Cliffs, New Jersey, 1991, Chapter 10, pages 177-202.	
		Jourdan et al, "eXtended Block Cache," Intel Corporation, Intel Israel, Haifa, 31015, Israel, pages 1-10.	
		McFarling, Scott, "Combining Branch Predictors," June 1993, WRL Technical Note TN-36, Digital Western Research Laboratory, Palo Alto, CA, 25 pp.	
		Michaud et al, "Exploring Instruction-Fetch Bandwidth Requirement in Wide-Issue Superscalar Processors," <i>Proceedings of the 1999 Int'l. Conference on Parallel Architectures and Compilation Techniques</i> , Oct. 12-16, 1999, Newport Beach, CA, pp. 2-10.	
		Patel et al, "Improving Trace Cache Effectiveness with Branch Promotion and Trace Packing," <i>Proceedings of the 25th Annual Int'l. Symposium on Computer Architecture</i> , June 27-July 1, 1998, Barcelona, Spain, pp. 262-271.	
		Reinman et al, "A Scalable Front-End Architecture for Fast Instruction Delivery," <i>Proceedings of the 26th Int'l. Symposium on Computer Architecture</i> , May 2-4, 1999, Atlanta, GA, pp. 234-245.	
		Rotenberg et al, "Trace Processors," <i>Proceedings of 30th Annual IEEE/ACM International Symposium on Microarchitecture</i> , December 1, 1997, Research Triangle Park, NC, pp. 138-148.	
		Seznec et al, "Multiple-Block Ahead Branch Predictors," <i>Proceedings of the 7th Int'l. Conference on Architectural Support for Programming Languages and Operating Systems</i> , Oct. 1-4, 1996, Cambridge, MA, pp. 116-127.	
		Yeh et al, "Increasing the Instruction Fetch Rate via Multiple Branch Prediction and a Branch Address Cache," <i>Proceedings of the 7th Int'l. Conference on Supercomputing</i> , July 1993, Tokyo, Japan, pp. 67-76.	

Examiner
SignatureDate
Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 808. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.